# Exhibit 19

# JEDEC STANDARD

## DDR4 SDRAM

## JESD79-4C

**(Revision of JESD79-4B, June 2017)**

**JANUARY 2020**

**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**

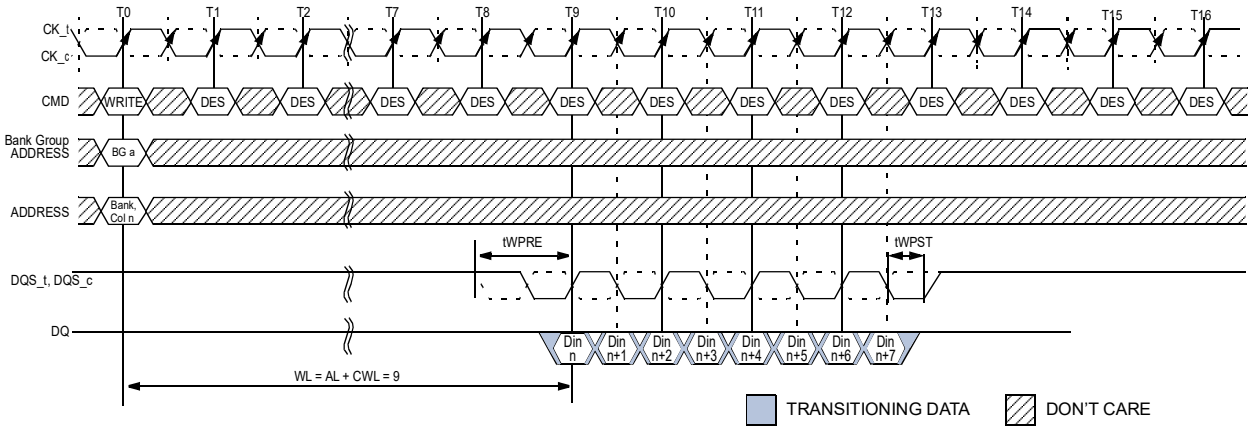
4.25.4 tWPST Calculation (cont'd)

**Table 84 — Timing Parameters by Speed Grade**

| Parameter | Symbol | DDR4-1600 | | DDR4-1866 | | DDR4-2133 | | DDR4-2400 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| DQS_t, DQS_c differential WRITE Preamble (1tCK Preamble) | tWPRE | 0.9 | - | 0.9 | - | 0.9 | - | 0.9 | - | tCK(avg) | |
| DQS_t, DQS_c differential WRITE Preamble (2tCK Preamble) | tWPRE2 | - | - | - | - | - | - | - | - | tCK(avg) | |
| DQS_t, DQS_c differential WRITE Postamble | tWPST | 0.33 | - | 0.33 | - | 0.33 | - | 0.33 | - | tCK(avg) | |
| DQS_t, DQS_c differential input low pulse width | tDQSL | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | tCK(avg) | |
| DQS_t, DQS_c differential input high pulse width | tDQSH | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | 0.46 | 0.54 | tCK(avg) | |
| DQS_t, DQS_c differential input high pulse width at 2tCK Preamble | tDQSH2PRE | - | - | - | - | - | - | - | - | tCK(avg) | |
| DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1tCK Preamble) | tDQSS | -0.27 | 0.27 | -0.27 | 0.27 | -0.27 | 0.27 | -0.27 | 0.27 | tCK(avg) | |
| DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge | tDSS | 0.18 | - | 0.18 | - | 0.18 | - | 0.18 | - | tCK(avg) | |
| DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge | tDSH | 0.18 | - | 0.18 | - | 0.18 | - | 0.18 | - | tCK(avg) | |

## 4.25.5 Write Burst Operation

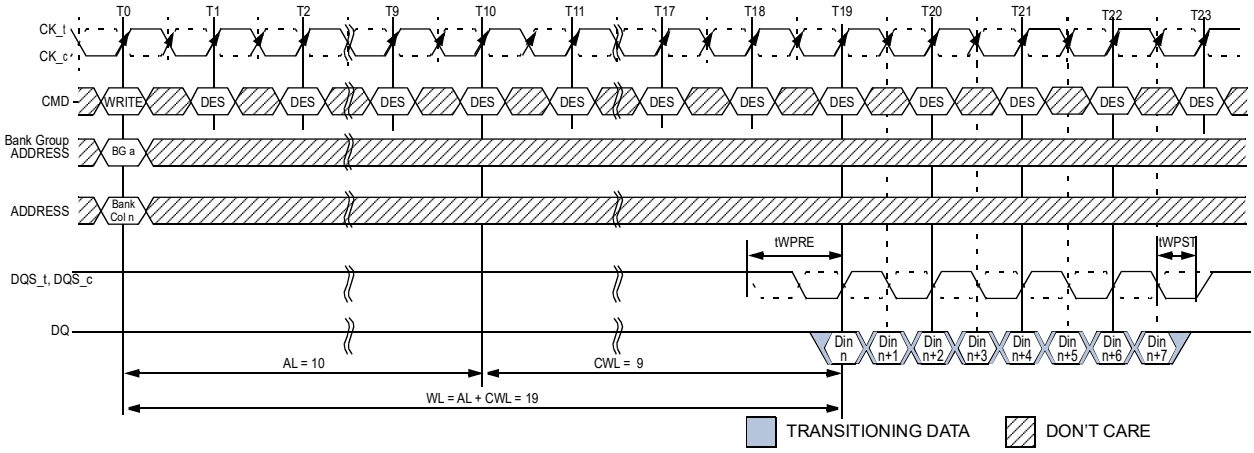
The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.




NOTE 1 BL = 8, WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
NOTE 2 DIN n = data-in to column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

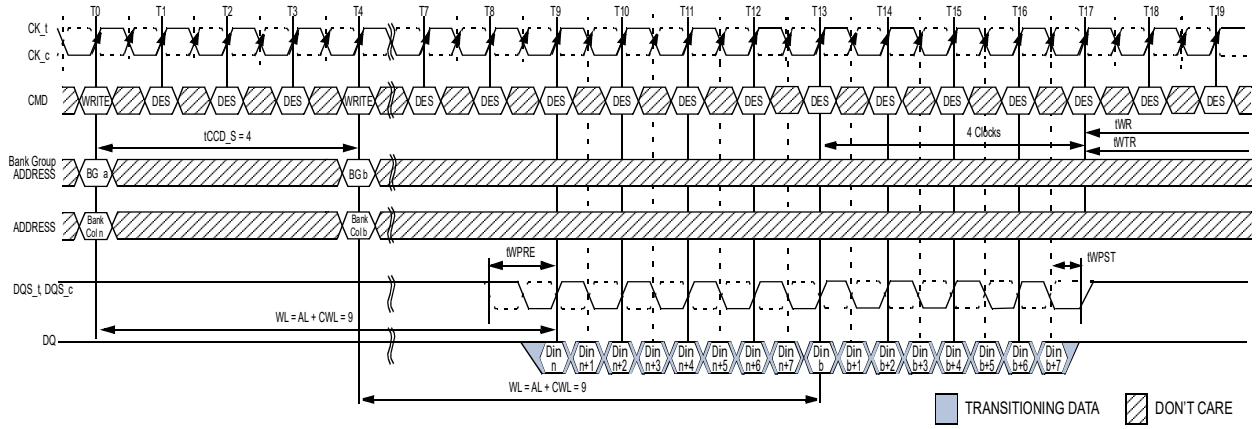
**Figure 128 — WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)**

4.25.5 Write Burst Operation (cont'd)




NOTE 1 BL = 8, WL = 19, AL = 10 (CL-1), CWL = 9, Preamble = 1tCK
NOTE 2 DIN n = data-in to column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

**Figure 129 — WRITE Burst Operation WL = 19 (AL = 10, CWL = 9, BL8)**




NOTE 1 BL = 8, AL = 0, CWL = 9, Preamble = 1tCK
NOTE 2 DIN n (or b) = data-in to column n (or column b).
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.
NOTE 5 C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable.
NOTE 6 The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

**Figure 130 — Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group**